IN THE CLAIMS

The following is a complete listing of the claims:

1. (currently amended) A programmable logic device comprising:

(currently amended) A programmable logic device comprising:

a programmable logic block including a plurality of macrocells, the macrocells operable to provide logical outputs at ~~its~~ the block's output terminals from logical inputs received at ~~its~~ the block's input terminals; and

a hardwired microsequencer coupled to the input and output terminals of the programmable logic block, the microsequencer operable to provide a sequence of logical inputs to the programmable logic block, at least part of the sequence determined by logical outputs ~~received from~~ provided by the macrocells of the programmable logic block.

2. (currently amended) The programmable logic device of claim 1, wherein the programmable logic block comprises a programmable AND array configured to provide a plurality of product terms based upon a set of logical inputs, and wherein the plurality of macrocells are operable to generate the logical outputs from the product terms.

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3. (original) The programmable logic device of claim 1, wherein the part of the set of logical inputs provided to the programmable logic block by the microsequencer are derived from microinstructions executed by the microsequencer.

4. (original) The programmable logic device of claim 2, wherein the microinstructions include an input, a jump destination, and a select command.

5. (currently amended) The programmable logic device of claim 1, wherein the microsequencer includes:

a memory configured to store a set of microinstructions that include at least some of the logical inputs provided to the programmable logic block; and

a program counter coupled to the memory and configured to provide addresses to the memory to select the microinstructions for execution, the program counter responsive to logical outputs received from the macrocells.

6. (original) The programmable logic device of claim 5, wherein the program counter is responsive to a jump destination derived from a previously executed microinstruction.

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7. (original) The programmable logic device of claim 5, wherein the memory is non-volatile.

8. (original) The programmable logic device of claim 5, wherein the microsequencer includes: a multiplexer having input terminals for receiving the logical outputs from the macrocells; an output terminal coupled to the program counter; and a select terminal coupled to an output terminal of the memory, the multiplexer responsive to a select command derived from a previously executed microinstruction.

9. (original) A method of sequencing a finite state machine, comprising:

generating input conditions for a finite state machine in a programmable logic block based upon a set of inputs;

selecting an input condition from the generated input conditions based upon a previously-executed microinstruction selected from a hardwired read-only memory;

selecting a microinstruction from a set of stored microinstructions in the read-only memory based upon the selected input condition and the previously-executed microinstruction; and

executing the selected microinstruction to provide inputs for the set of inputs.

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10. (original) The method of claim 9, wherein the selecting a microinstruction act comprises:

if the selected input condition is in a first binary state, selecting the microinstruction at a jump destination derived from the previously-executed microinstruction; and

if the selected input condition is complementary to the first binary state, selecting the microinstruction according to a predetermined microinstruction sequence.

11. (original) The method of claim 10, wherein the executing the microinstruction act includes determining the first binary state.

12. (original) The method of claim 9, wherein the programmable logic block comprise a programmable AND array, and the generating input conditions act comprises processing product terms through the programmable AND array.

13. (currently amended) A programmable logic device, comprising:

a logic block <u>including a plurality of macrocells, the macrocells</u> operable to provide input conditions for a finite state machine based upon a set of inputs; and

a hardwired microsequencer configured to determine a next state of the finite state machine by cyclically executing a

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microinstruction selected from a set of microinstructions responsive to cycles of a system clock, wherein at a given cycle of the system clock, the executed microinstruction depends upon the previously-executed microinstruction and an input condition selected from the input conditions provided by the macrocells of the logic block, and wherein the set of inputs for the logic block includes inputs derived from the executed microinstruction.

14. (original) The programmable logic device of claim 13, wherein the hardwired microsequencer includes:

a sequence memory configured to store the set of microinstructions; and

a program counter configured to determine the microinstruction to be executed at each internal clock cycle, wherein depending upon the selected input condition, the program counter determines the microinstruction either according to a predetermined sequence of the microinstructions or to a jump destination derived from the previously-executed microinstruction.

15. (original) The programmable logic device of claim 14, wherein the sequence memory is a read-only memory.

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16. (original) The programmable logic device of claim 14, wherein the sequence memory is a non-volatile electrically-alterable read-only memory.

17. (original) The programmable logic device of claim 14, wherein the hardwired microsequencer further includes a multiplexer configured to select from the input conditions provided by the logic block and determine the selected input signal according to a condition selection command derived from the previously-executed microinstruction.

18. (currently amended) The programmable logic device of claim 14, wherein the program counter is configured to determine the microinstruction according to the jump destination if the selected input condition is in a first binary state and wherein the program counter is configured to determine the microinstruction according to the predetermined sequence if the selected input condition is in the complementary binary state to the first binary ~~state~~ state.

19. (original) The programmable logic device of claim 18, wherein the first binary state is determined by the previously-executed microinstruction.

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20. (original) The programmable logic device of claim 18, wherein the hardwired microsequencer further includes:

a multiplexer configured to select from the input conditions provided by the logic block and determine the selected input signal according to a condition selection command derived from the previously-executed microinstruction; and

an exclusive OR gate configured to receive the selected input signal from the multiplexer and a binary state selection command derived from the previously-executed microinstruction to determine the first binary state.

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